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Product Specification

1.8″ COLOR TFT-LCD MODULE

MODEL NAME: A018AN03 V1

< >Preliminary Specification

<◆> Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0	09/May/2002		First draft.
1	27/May./2002	15	Revised the error
		17	Revised the error
		18	Add the extraction block of display data
2	31/May/2002	7	V_{CAC},V_{GL-AC}: 5.2V→5.6V
		8	Dc-Dc block Output voltage: 13V→13.5V; Vref: 1.25V→1.2V
		12	Add FPC reliability test item
		13	Update outline drawing
		21	Updated R.C parameter
		22	Cosmetic specification included
3	31/Oct/2002	6	Vcom from 5.2 to 5.6
		7	V_{GL_H} from –10 to –7.1
		8	Delete data set-up time and data hold time on table and Tc à Tvc
		9	Delete sel0 sel1 in note fo drawing
		18	Hsync CLK 1560 à360
		19	Modify drawing (pixel arrangment)
4	03/Dec/2002	20	Modify drawing
5	09/Dec/2002	5	Correct note 4
		7	Remove LED typical voltage and add LED maximum voltage
6	07/Apr/2003	2	Revised the footnote
		5	Modify drawing(BOTTEN àBOTTOM)
		5	Add Note 6

		4	Add Note 6 to Pin assignment 13:SHDB
		5	Add Note 6 to Pin assignment 28:GRB
		7	Add output signal voltage H leavel: V_{OH} MAX:V_{CC}
		8	Add DCLK Frequency MAX:6.0, Min:5.37
7	15/May/2003	22	Correct Fig.22 Application circuit R112 **à** OPEN, R111 **à** 10K
8	20/Jun/2003	7	Add “Customer can ignore the power-up sequence if connecting GRB to LCD backlight control signal, LCD_BL” in Note 5; change the 2nd Note 5 to Note 7.
		8	Remove Vcom in Table 3, Absolute Maximum Ratings
		9	Add AVDD1=4.0V(min), 5.6V(Typ), and 6.0V(Max) in Table a; add Note 5
		9	Add I_{DD1} =0.5mA(Typ), and 0.7mA(Max) in Table b.

Contents:

Appendix:

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution(dot)	280(W) ×220(H)	
2	Active area(mm)	35.6(W) ×26.6(H)	
3	Screen size(inch)	1.75(Diagonal)	
4	Dot pitch(mm)	0.127(W) ×0.121(H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension(mm)	48.6(W) ×39.8(H) ×3.9(D)	Note 1
7	Weight(g)	12.6± 2 typ.	
8	Panel surface treatment	Hard coating (3H)	

Note 1: Refer to Fig. 4

B. Electrical specifications

1.Pin assignment

a. TFT-LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	GND	-	Ground for gate	
2	V_{CC}	P	Supply voltage of logic control circuit for scan driver	
3	V_{GL}	P	Negative power for scan driver	
4	V_{GH}	P	Positive power for scan driver	
5	FRP	O	Gate driver input signal that is frame polarity output for Vcom	
6	VCOM	I	Common electrode driving signal	
7	DRV	VO	Power transistor gate signal for the boost converter	
8	GND	-	Ground	
9	FB	VI	Main boost regulator feedback input(FB threshold is 1.2V)	
10	SHL	I	Left/Right scan control input	Note 1
11	STB	I	Stand by mode setting pin.	Note 2
12	V_{CC}	P	Supply voltage for source driver	
13	SHDB	I	Shutdown input. Active low.	Note 3 Note 6
14	AGND	P	Ground pins for analog circuits	
15	VLED	I	LED Anode	
16	GLED	O	LED Cathode	
17	AVDD	P	Power supply for analog circuits	
18	HSYNC	I	Horizontal sync input. Negative polarity	
19	VSYNC	I	Vertical sync input. Negative polarity.	
20	DCLK	I	Clock signal; latch data onto line latches at the rising edge.	
21	D07	I	Data input. :MSB	
22	D06	I	Data input	
23	D05	I	Data input	
24	D04	I	Data input	
25	D03	I	Data input	

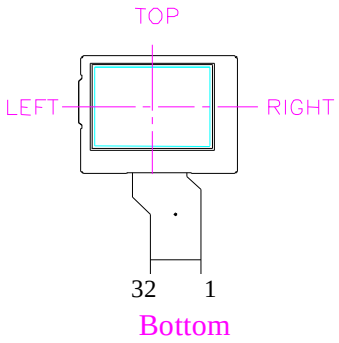
26	D02	I	Data input. :LSB	
27	SEL0	I	Select pin for interface definition	Note 4
28	GRB	I	Global reset pin.	Note 5 Note 6
29	U/D	I	Up/Down scan control input	Note 1
30	GND	-	GND for logic circuit	
31	AVDD1	P	Supply of positive power for level shift circuit.	
32	AGND1	P	Ground for level shift circuit	

I: Input; O: Output. VI: voltage input VO: voltage output P:power

Note 1: Selection of scanning mode

Mode	**Setting of scan control input**		**Scanning direction**
	U/D	SHL	Note 5
Normal mode	L	H	From up to down, and from left to right.
Reverse mode	H	L	From down to up, and from right to left.

Refer to figure as below:



Note 2: Stand by mode(STB).If STB high, it is normal operation.
If it is low, it is standby function. Normally pulled high.

Note 3:Shutdown input(SHDB).Active low, DC-DC converter is off when SHDB is low, Normally pulled low.

Note 4: interface select pin, Pull Low for UPS051 interface.

Note 5:Global reset pin. It should be connected to VCC in normal operation. If Connected to GND, the controller is in reset state, normally pulled high. Customer can ignore the power-up sequence if connecting GRB to LCD backlight control signal, LCD_BL.

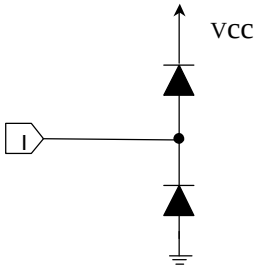
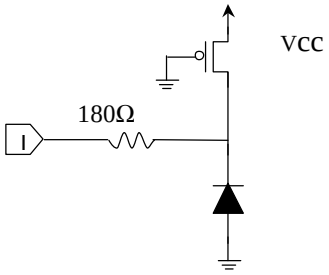
Note 6:Be sure to apply GRB to low and SHDB to low first, before turn off DCLK.

Note 7: Definition of scanning direction.

b. LED driving section (Refer to Fig.1)

No.	Symbol	I/O	Description	Remark
Pin15	VLED	I	LED Anode	
Pin 16	GLED	-	LED Cathode	

2. Equivalent circuit of I/O

Pin no & Pin name	Schematics
7.DRV	
8.FB 9 SHL 10.STB 12.SHDB 17.HSYNC 18.VSYNC 19.DCLK 20.D07 21.D06 22.D05 23.D04 24.D03 25.D02 26.GRB 27.U/D	

3. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{CC}	GND=0	-0.5	5.	V	
	AV_{DD}	AV_{SS}=0	-0.5	5.5	V	
	V_{GH}	GND=0	-0.3	21	V	
	V_{GL}		-17	0.3	V	
	$V_{GH}-V_{GL}$		-	38	V	
Operating temperature	Topa		0	60	℃	Ambient temperature

Storage temperature	Tstg		-25	80	℃	Ambient temperature

4. Electrical characteristics

a. Typical operating conditions (GND=AVss=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		V_{CC}	2.5	3.3	3.6	V	
		AV_{DD}	3.2	3.3	4.5	V	
		AV_{DD1}	4.0	5.6	6.0	V	Note 5
		V_{GH}	14	16	18	V	
		V_{GL_AC}	-	5.6	-	Vp-p	AC component of V_{GL}. Note 1
		V_{GL_H}	-13.5	-11.5	-9.5	V	High level of V_{GL}.
VCOM		V_{CAC}	-	5.6	-	Vp-p	AC component, Note 2
		V_{CDC}	0.1	0.5	0.8	V	DC component, Note 3 Note 4
Output Signal voltage	H Level	V_{OH}	Vcc-0.4		Vcc	V	
	L Level	V_{OL}	GND		GND+0.4	V	
Input Signal voltage	H Level	V_{IH}	$0.7V_{CC}$	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	$0.3V_{CC}$	V	
DRV output voltage		V_{DRV}	0		VCC	V	
DRV output		IDRV			10	mA	
Feedback voltage		V_{FB}		1.2	1.25	V	
Output current	H Level	IOH		10		uA	
	L Level	IOL		-10		uA	
Analog stand by current		Ist			200	uA	DCLK is stopped
FRP output current		H Level	I_{OHF}		20	mA	For Vcom circuits.
		L Level	I_{OLF}		20	mA	

Note 1: The same phase and amplitude with common electrode driving signal (VCOM).

Note 2: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.

Note 3: V_{CDC} could be adjusted so as to minimize vertical straight line, flicker and maximum contrast on each module.

Note 4: Be sure to apply GND, V_{CC} and V_{GL} (V_{GL} must lower than 0 volt) to the LCD first, and then apply V_{GH}.

Note 5: AVDD1 is supply voltage for VCOM swing circuit, this circuit output FRP signal. The voltage will decide VCOM peak to peak value,(and VCOM peak to peak is 5.6V).

Note 6: The applicable pins are SHL, STB, SHDB, HSYNC, VSYNC, DCLK, D05~D00,GRB,U/D :

b. Current consumption (GND=AVss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark

Current for driver	I_{GH}	V_{GH}=14.7V	-	0.25	1.0	mA	
	I_{GL}	V_{GL_H}=-11V	-	-0.14	-0.8	mA	
	I_{CC}	V_{CC}=3.3V	-	3.0	6	mA	
	I_{DD}	AV_{DD}=3.3V	-	1.5	3	mA	
	I_{DD1}	AV_{DD1}=5.6V	-	0.5	0.7	mA	

c. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current			20		**mA**	
LED voltage	V_L			***12***	***V***	
LED Life Time	L_L	10000			Hr	Note 1,2

Note 1 : Ta. = 25℃, I_L = 20mA
Note 2 : Brightness to be decreased to 50% of the initial value.

5. AC Timing

a. Timing conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK	Frequency	1/Tvc	5.37	5.67	6.0	MHz	
	High time	Tvch	15			ns	
	Low time	Tvcl	15			ns	
Rising time		t_r	-	-	10	ns	Note 1
Falling time		t_f	-	-	10	ns	Note 1
HSYNC	Period	TH	60	63.56	67	us	Note 2
				360		DCLK	
	Display period	THd		49.4		us	
	Pulse width	THp	1	25		DCLK	
	HSYNC-Clk timing	THc	15		Tvc-15	ns	
Hsync setup time		Tvst	12			ns	
Hsync hold time		Thhd	12			ns	
Horizontal lines per field		t_V	256	262	268	t_H	
VSYNC	Period	TV		16.6		ms	Note 2
				262		t_H	
	Display period	TVd		13.97		ms	
	Pulse width	TVp	1			DCLK	
				3		TH	
Vsync setup time		Tvst	12			ns	
Vsync hold time		Tvhd	12			ns	
DATA D00~D05	DCLK-DATA timing	Tds	10	-	-	ns	
	DATA-CLK timing	Tdh	10	-	-	ns	

	Rising time Falling time	Tdrf	-	-	10	ns	

Note 1: For all of the logic signals.

Note 2: Display position

A.. Horizontal display position

The display starts from the data of (57DCLK, THe=57DCLK) as shown in Fig 5.

(THe : From Hsync falling edge to 1st displayed data.)

B. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		25		TH	NTSC

b. Timing diagram

Please refer to the attached drawing, from Fig.5 to Fig.8.

6. DC-DC Converter Circuit

A018AN03 V1contains one high-power step-up DC-DC converter, and backplane drive circuitry for active matrix TFT LCDs. The output voltage of the main boost converter can be set from VCC to 13.5V with external resistors. Also included in A018AN03 V1 are a precision 1.2V reference voltage, fault detection and logic shutdown.

a .Boost Converter

A018AN03 V1 main boost converter uses a boost PWM architecture to produce a positive regulated voltage, Please refer to the below figures to see the block diagram.

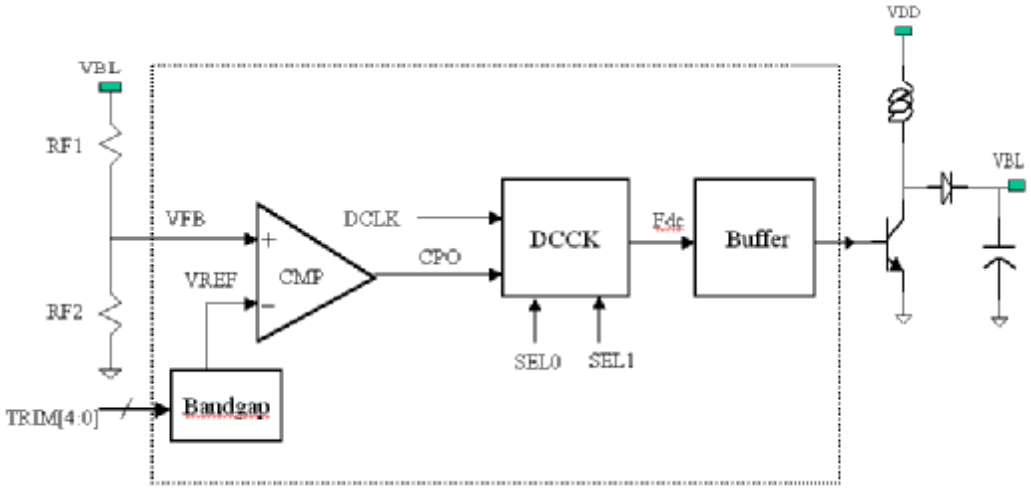


Fig 1 DC-DC converter block diagram

In the internal architecture of DC-DC converter. The feedback voltage(VFB) will connect to the tri-angle waveform comparator ,and generates the output signal (CP0) which determines the duty cycle for (Fdc).

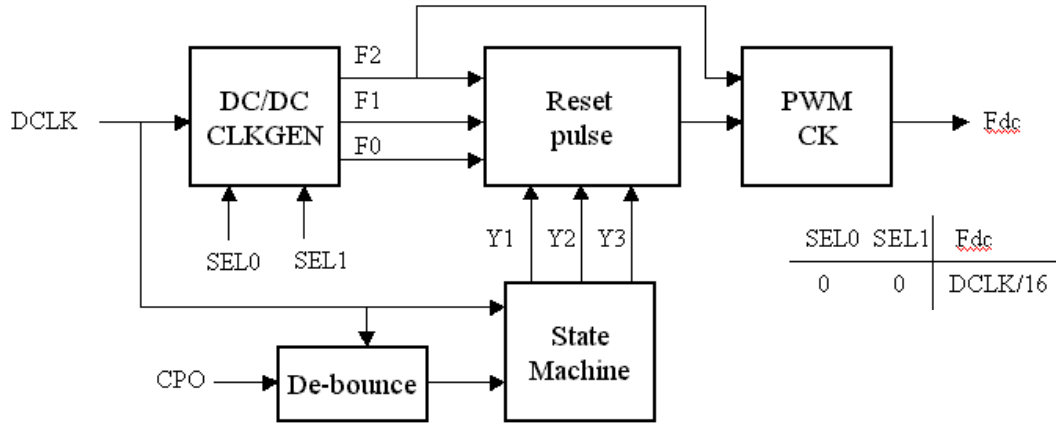


Fig 2 DCCK block diagram

To reduce the noise affect,CP0 will processed by De-bounce circuit. State-machine will generate the duty cycle by CP0 signal. To make sure that VFB can reach default VREF quickly, so State-machine's is designed as a discrete step by step function. please refer to Fig 3. If CP0 is low , Duty cycle will work from 0% to 75%. The maximum duty ratio is 75%.

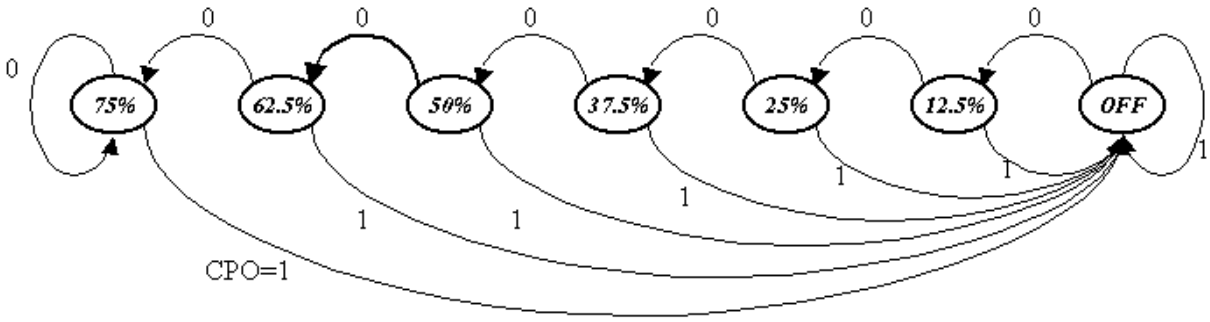


Fig 3 PWM Control state diagram

b.Shutdown Mode

In shutdown mode, a logic-low level on SHDB, pwm controller and the reference are disabled. The supply current drops to maximize battery life and the reference is pulled to ground. Every output voltage will decay. If unused, connect SHDB to VCC.

c.Oscillator Circuit

The boost-converter operating frequency was set at 1/16 times the system clock, DCLK. In A018AN03 V1's model. the DC-DC converter osc frequency is DCLK/16=354.4khz

C. Optical specification (Note 1,Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time Rise Fall	 Tr Tf	 θ =0°	 - -	 25 30	 50 60	 ms ms	Note 4
Contrast ratio	CR	At optimized viewing angle	60	150	-		Note 5,6
Viewing angle Top Bottom Left Right		CR≧10	 10 30 40 40	 - - - -	 - - - -	deg.	Note 7
Brightness	Y_L	θ =0°	*180*	240	-	cd/m^2	Note 8
White chromaticity	X	θ =0°	0.26	0.31	0.36		
	y	θ =0°	0.29	0.35	0.40		

Note 1. Ambient temperature =25℃. And backlight current I_L=*20 mA*

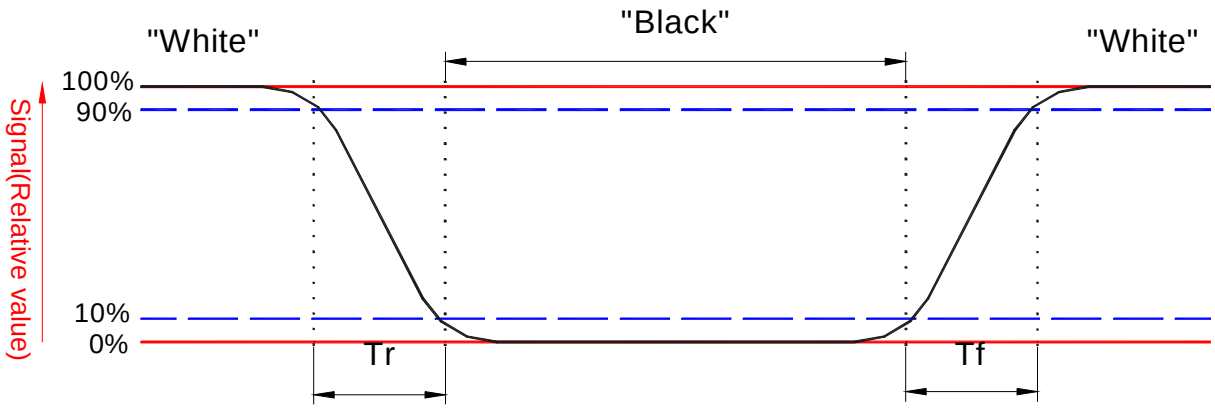
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

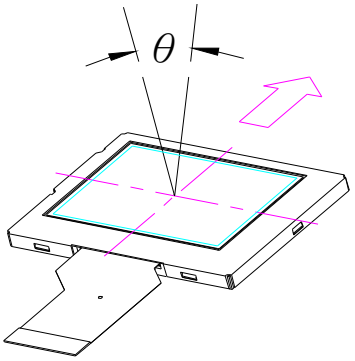
Contrast ratio is calculated with the following formula.

Contrast ratio (CR)= Photo detector output when LCD is at “White” state

Photo detector output when LCD is at “Black” state

Note 6. White Vi=V_{i50} $\overline{+}$ 1.5V
Black Vi=V_{i50} ± 2.0V
“±” Means that the analog input signal swings in phase with COM signal.
“$\overline{+}$” Means that the analog input signal swings out of phase with COM signal.
V_{i50} : The analog input voltage when transmission is 50%
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:, refer to figure as below.



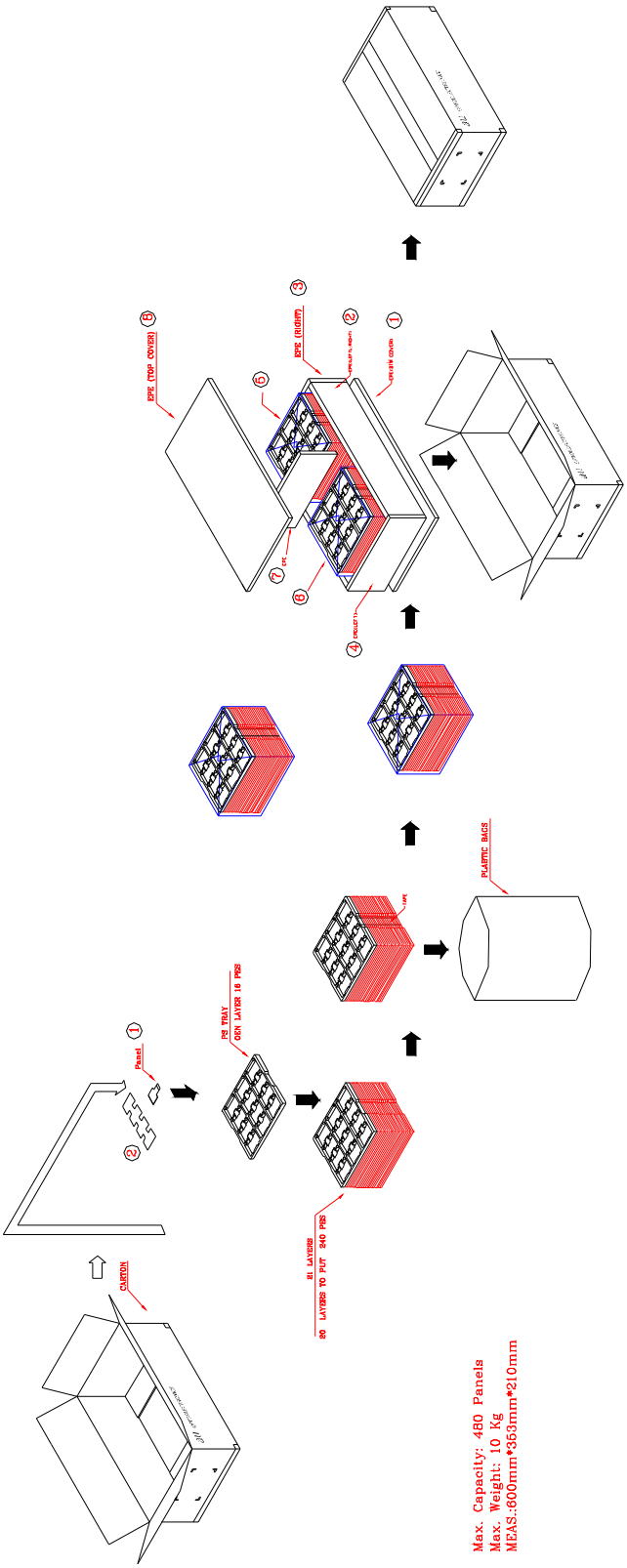
Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

D. Reliability test items:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	
12	The copper's strength for FPC	The strength is larger 0.7 kg/cm	IPC TM650
13	The film's strength for FPC	The strength is larger 0.35 kg/cm	IPC TM650
14	Flexible ability for FPC	1. curved radius: 2mm 2. curved angle: 270° 3. Pulling force: 500g	MIT folm: Diagram of test set up for folding endurance

Note: Ta: Ambient temperature.

E. Packing form



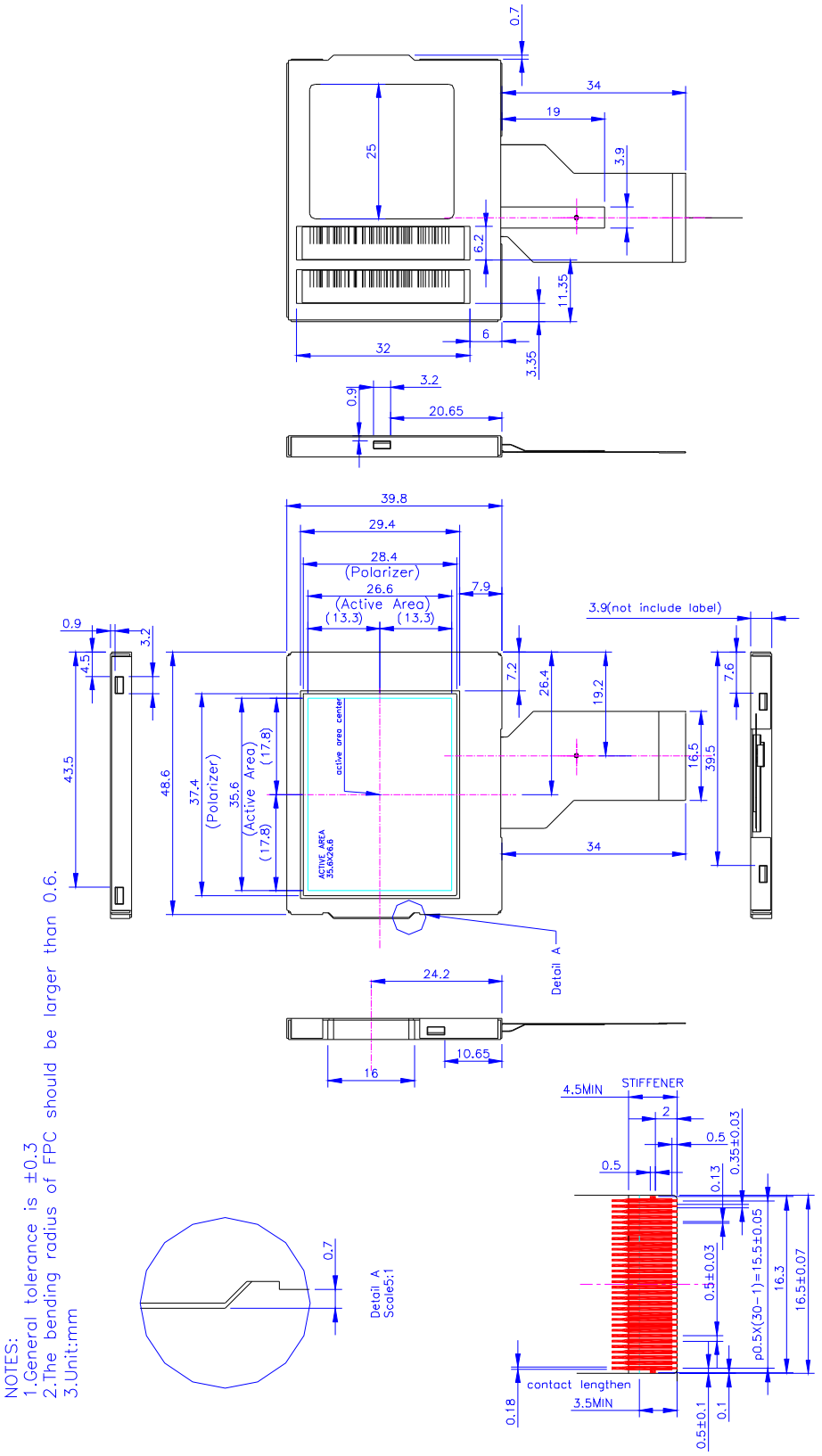


Fig. 4 outline dimension of TFT-LCD module

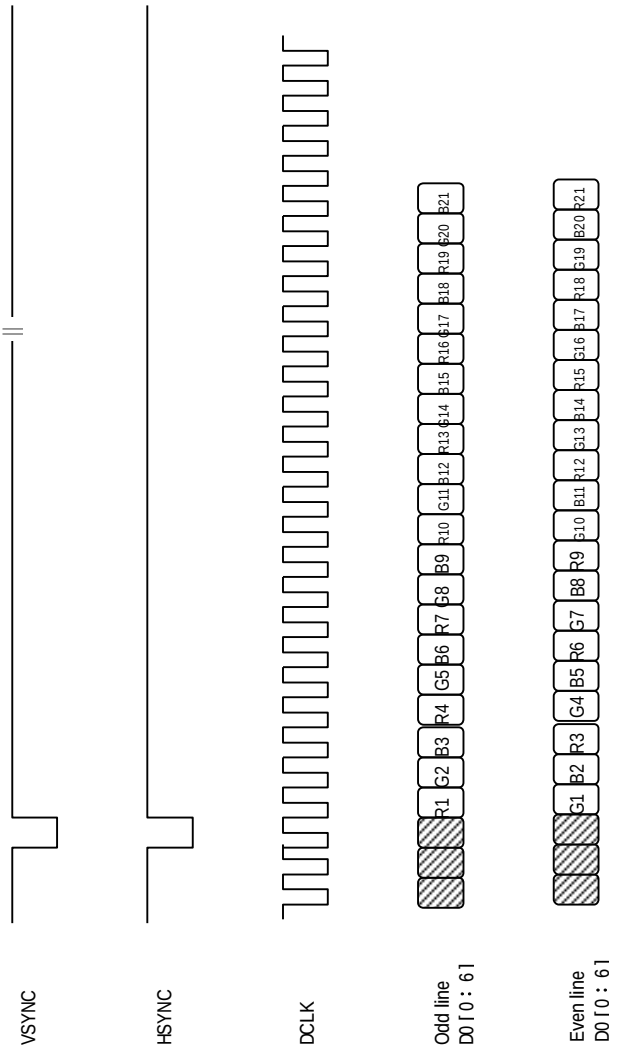


Fig. 5 Input signals timing relationship

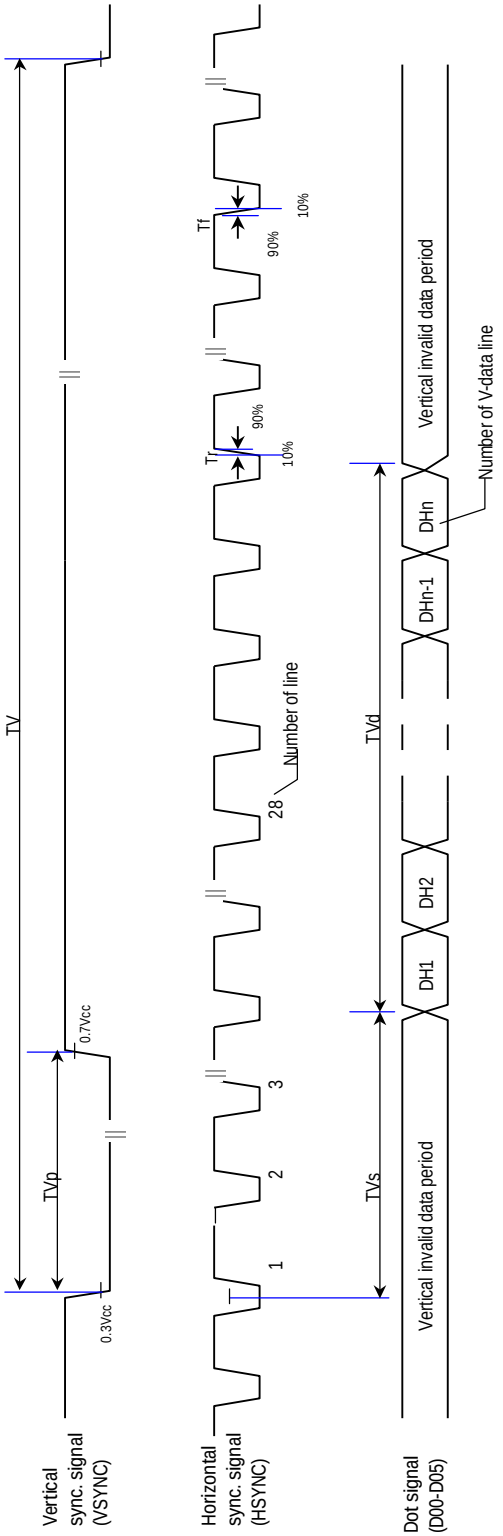


Fig. 6 Input Vertical Timing

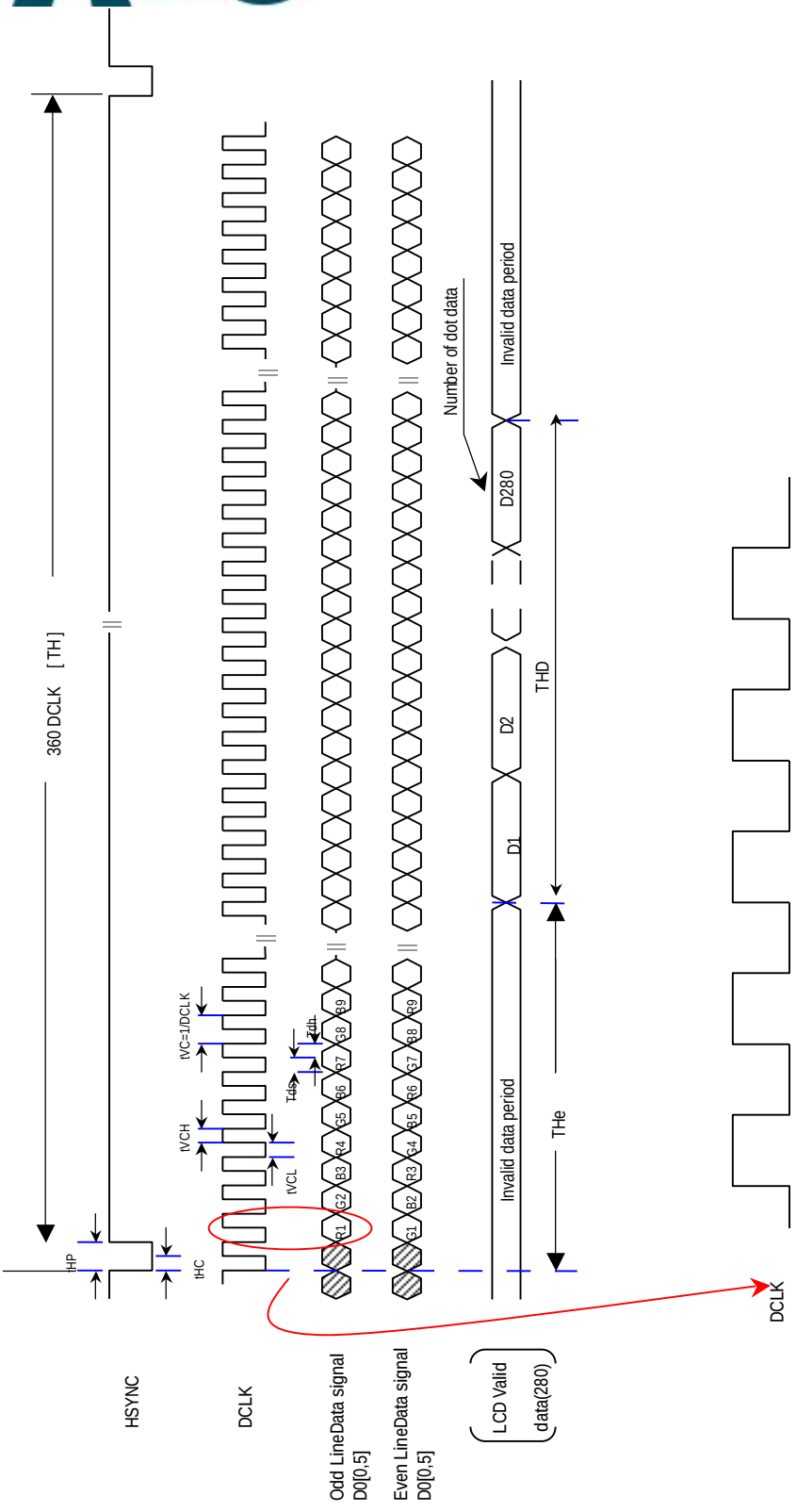


Fig. 7 Horizontal Input Timing)

Fig. 8 Extraction of display data from memory to panel

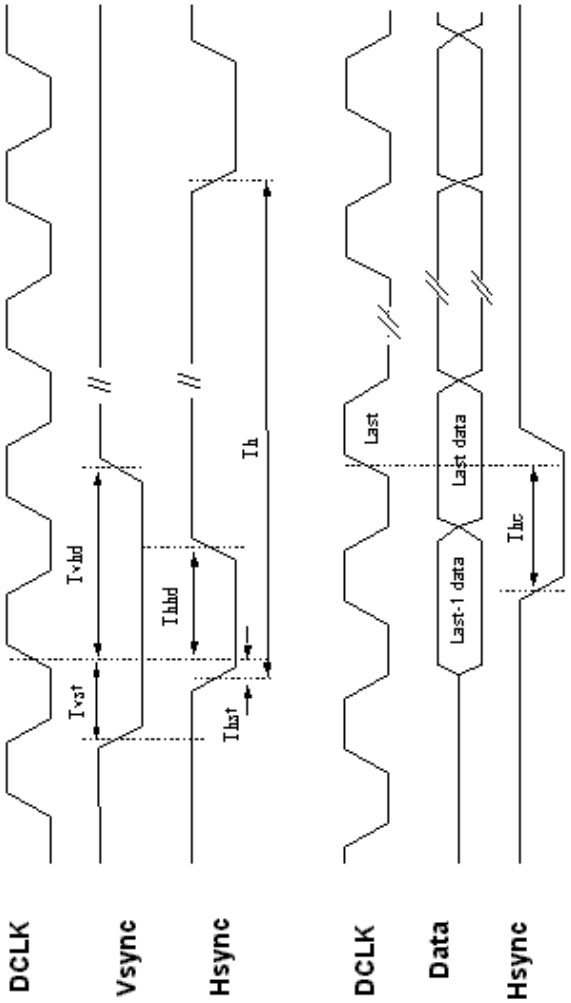


Fig. 9 Hsync, Vsync, Data, DCLk relationship

Application Circuit

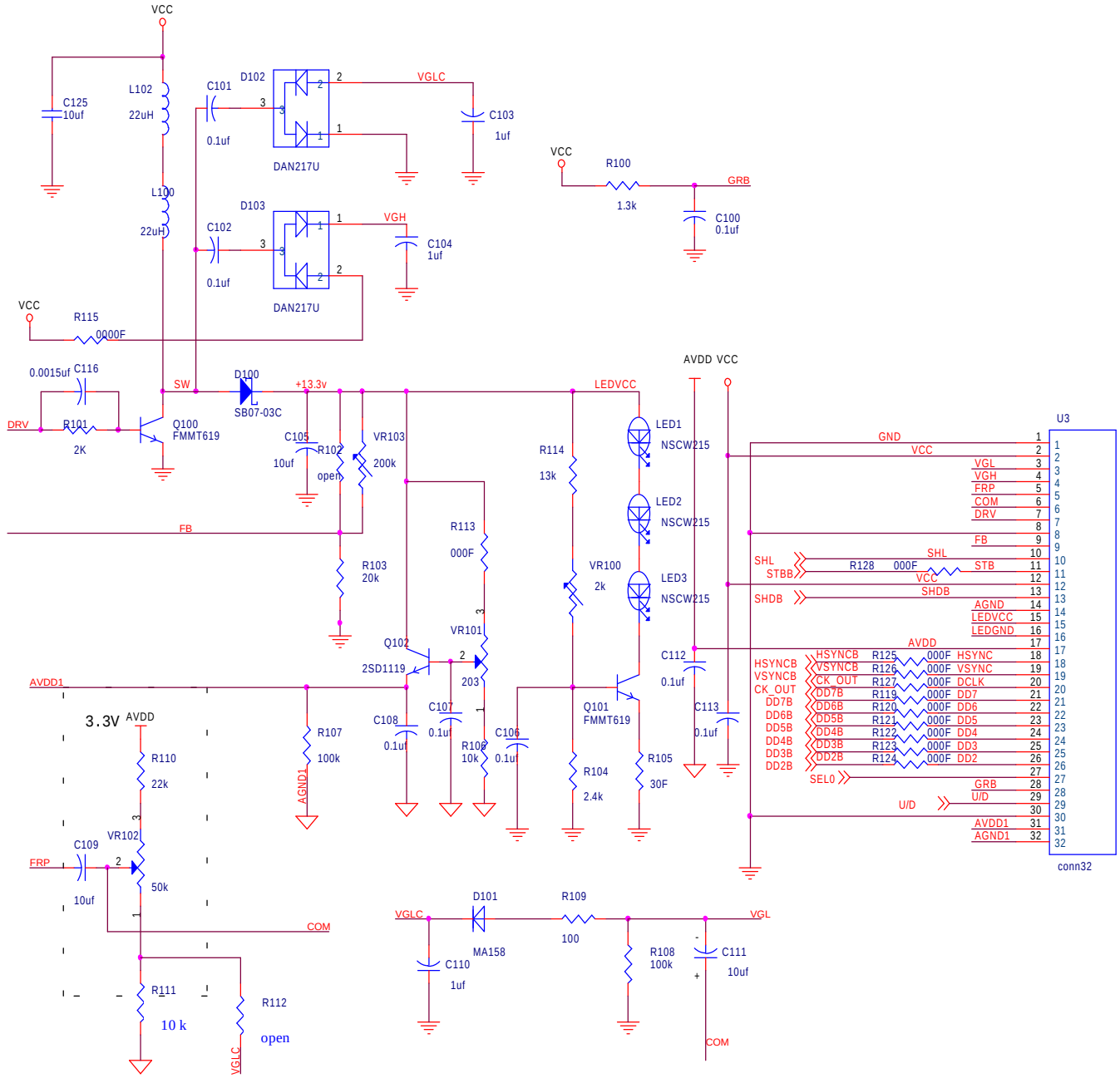


Fig. 10 Typical application circuit (for reference)